

SINGLE-POLY 2-TRANSISTOR BASED FUSE ELEMENT**BACKGROUND OF THE INVENTION**5 Technical Field of the Invention

The invention relates generally to the field of integrated circuit and, more particularly, to fusible link programming in semiconductor integrated circuits.

Description of Related Art

10 In integrated circuits including CMOS integrated circuits, it is often desirable to be able to permanently store information, or to form permanent connections of the integrated circuit after it is manufactured. Fuse or anti-fuse devices forming fusible links are frequently used for this purpose. Fuses and anti-fuses can also be used to program redundant elements to replace identical defective elements such as DRAM, Flash EEPROM, SRAM, or other
15 memories. Further, fuses can be used to store die identification or other such information, or to adjust the speed of a circuit by adjusting the resistance of the current path.

One type of fuse device is "programmed" or "blown" using a laser to open a link after a semiconductor device is processed and passivated. This type of fuse device requires precise alignment of the laser on the fuse device to avoid destroying neighboring devices.

20 This and other similar approaches can result in damage to the device passivation layer, and thus, lead to reliability concerns. For example, the process of programming the fuse can

cause a hole in the passivation layer when the fuse material is displaced. Also the method is not in-system, sometimes inconvenient, and thus lead to higher test cost.

Another type of fuse device is the electrical fuse/anti-fuse. Electrical fuse/anti-fuses have been introduced into semiconductor products and are, in many applications, replacing the commonly used laser fuses. The typical electrical fuse/anti-fuse is in-system but is one-time programmable. It is generally a passive element such as resistor or capacitor which is programmed or blown using electrical pulses via a programming (pass gate) transistor. Since significant energy or high programming current is required to pass through these devices to reach the passive element, the size required for the programming (pass gate) transistors can be very large.

For example, a currently used anti-fuse device is structured based on a conventional MOS transistor. Such an anti-fuse is programmed by applying a voltage (generally about 7 Volts) across the gate-oxide of the MOS transistor. The programming process results in a damaged gate-oxide which reduces the electrical resistance across the oxide. A sensing circuit attached to the anti-fuse is used to differentiate between the high resistance of the intact oxide and the lowered resistance of the damaged oxide. For lower resistances and more reliable sensing, even higher programming voltages and programming currents are used.

Because of the significant energy required for programming, damage can result to surrounding structure and/or unreliable sensing can result because of the inconsistent nature of the blow process and the relatively small change typically offered in the programmed

resistance. Further, these type of devices may not be viable for use with many of the latest process technologies because of the required programming potentials, i.e. high current flow and high voltage levels over a requisite amount of time. It would be advantageous to lower the programming parameters in order to enable reduction of the size of the associated circuits (e.g. voltage generator, programming transistor, wiring, etc.) and/or improve the sensing reliability.

SUMMARY OF THE INVENTION

The present invention achieves technical advantages as an electrically programmable transistor fuse having a source and drain disposed in a semiconductor substrate and further having a double-gate arrangement disposed in a single layer of polysilicon in which one gate is capacitively couple to the drain region. The transistor fuse further includes a coupling device adapted to increase the capacitive coupling of the one gate and the drain region for enabling reduction in fuse programming voltage, wherein programming of the transistor fuse is effectuated via application of a voltage signal to the drain in which the voltage signal is less than the junction breakdown of the transistor fuse.

10

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, reference is made to the following detailed description taken in conjunction with the accompanying drawings wherein:

Figure 1 illustrates a conventional EEPROM device;

5 Figure 1A illustrates an circuit equivalent of a series-connected isolation transistor and a floating gate transistor;

 Figures 2A illustrates a 2-transistor structure for use as an electrical fuse element in accordance with exemplary embodiments of the present invention;

 Figure 2B illustrates a top view of the 2-transistor structure shown in Figure 2A;

10 Figure 3A illustrates another 2-transistor structure for use as an electrical fuse element in accordance with exemplary embodiments of the present invention;

 Figure 3B illustrates a top view of the 2-transistor structure shown in Figure 3A;

 Figure 4A illustrates still another 2-transistor structure for use as an electrical fuse element in accordance with exemplary embodiments of the present invention;

15 Figure 4B illustrates a top view of the 2-transistor structure shown in Figure 4A;

 Figure 5A shows a diagram illustrating programming of the 2-transistor structures illustrated in Figures 2A, 3A, and 4A;

 Figure 5B shows biasing for the 2-transistor structures illustrated in Figures 2A, 3A, and 4A;

20 Figure 6A illustrates a fuse cell in accordance with exemplary embodiments of the present invention;

Figure 6B shows biasing for the fuse cell illustrated in Figure 6A; and

Figure 7 illustrates a fuse array in accordance with exemplary embodiments of the present invention.

DETAILED DESCRIPTION

The numerous innovative teachings of the present application will be described with particular reference to the presently preferred exemplary embodiments. However, it should
5 be understood that this class of embodiments provides only a few examples of the many advantageous uses and innovative teachings herein. In general, statements made in the specification of the present application do not necessarily delimit any of the various claimed inventions. Moreover, some statements may apply to some inventive features, but not to others. Throughout the drawings, it is noted that the same reference numerals or letters will
10 be used to designate like or equivalent elements having the same function. Detailed Descriptions of known functions and constructions unnecessarily obscuring the subject matter of the present invention have been omitted for clarity.

Current electrical fuses are passive elements, such as resistors or capacitors, which are programmed by electrical pulses with typical programming currents in the order of milli-
15 amp (mA) or transistor fuses having programming voltage greater than the junction breakdown of the transistor. In accordance with exemplary embodiments of the present invention, a single polysilicon 2-transistor EEPROM type transistor advantageously realized in a self-aligned CMOS process is described and used as a fuse element. The programming current required to program a 2-transistor EEPROM type device is in the order of few micro-
20 amp (μ A), a three order of magnitude reduction over typical electric type fuses. However,

conventional EEPROM devices are not CMOS compatible and have high programming potentials.

Conventional split-gate EEPROM structures are formed using at least two layers of polycrystalline silicon and include a floating gate transistor as shown in Figure 1. This memory cell configuration is equivalent to a series connected isolation transistor 11 and floating gate transistor 12 as illustrated in the circuit diagram of Figure 1A. The isolation transistor 11 is not influenced by the state of the floating gate and will remain off when its control gate is not activated. For this conventional memory structure, the first layer of poly forms the floating gate. The floating gate covers a portion of a channel region between the source and drain. The remainder of the channel region is directly controlled by a second layer of poly, the control gate, which overlies the floating gate. This overlying control gate couples the gate voltage onto the floating gate and helps pull-up the channel hot electrons. The negative charges injected to the floating gate changes the V_t of the transistor since the trapped electrons change the gate work function; thus requiring additional gate voltage to turn on the device.

Although this conventional floating gate structure works well for many memory devices, it deviates from the conventional (single poly) CMOS process; thus requiring additional process steps as well as increasing process complicity in deposit and removal of the floating gate poly in a small density area among a large processor chip. Also, the floating gate poly presents added equipment costs to maintain compatibility among logic Fabs, for the conventional logic CMOS Fab is equipped with single poly process.

Referring now to Figures 2A, 3A, and 4A there are illustrated 2-transistor structures for use as an electrical fuse element (eFuse) in accordance with exemplary embodiments of the present invention. In each illustrated structure, the control gate and floating gate are implemented in a single-poly process using standard CMOS processing without adding another polysilicon level. Single poly enables the eFuse to be implemented in a host logic process preserving the same process steps maintaining process simplicity and process cost. In addition, the 2-transistor structures of Figures 2A, 3A, and 4A operate at a much lower programming voltage because the gate voltage (~5V or below) is enabled to serve to turn on the 2-transistor portion. A vast improvement to the gate bias for programming (~12V) for the structure shown in Figure 1 and other similar memory devices requiring such a high programming voltage. The typical operating bias for the conventional structure of Figure 1 is shown in tabular format in Figure 1B.

Referring now to Figures 2A and 2B, the eFuse 200 includes a source region 210 and drain region 211 of a first conductivity type formed in a semiconductor substrate of a second conductivity type opposite from the first conductivity type in which the source 210 and drain 211 are spaced apart to define a channel region 213 therebetween. Formed over the source region 210, drain region 211 and channel region 213 is a uniform layer of insulating material, on the order of 50nm. The eFuse 200 further includes a 2-transistor arrangement formed in a single layer of poly. The 2-transistor includes a floating gate portion 215 overlapping a portion of the drain 211 and a control gate portion 216 overlapping a portion of the source 210. The control gate 216 includes a terminal for receiving externally applied

voltage potentials for controlling programming and read operations. The floating gate portion 215 and a control gate portion 216 are isolated from one another. Further, an isolated well region 220 can also be formed in the semiconductor substrate. Figure 2B illustrates a top layout view of the eFuse shown in Figure 2A. The isolated well 220 is drawn in the semiconductor substrate to overlap only the floating gate portion 215 providing for increased capacitive coupling and reduced programming voltage.

In operation, biasing of the eFuse is achieved through capacitive coupling. That is, the floating gate 215 is independently biased via capacitive coupling with the drain 211 and isolated well 220. The floating gate 215 is charged using programming known as Channel Hot Electron programming. In particular (as is illustrated in Figure 5A and 5B), with the source 210 grounded (V_{ss}), threshold voltage (V_t) applied to the gate, and a programming voltage applied to the drain 211, a programming current flows and electrons are provided by source side injection to the floating gate 215 when sufficient energy is gained to jump the silicon energy barrier ($\sim 3.1\text{eV}$). The isolation well 220 and an extended RX width drain (further discussed below) are designed to provide at least a 70% coupling between the drain 211 and floating gate 215 to enable the lower programming voltage thus, no HV process is needed. With this transistor structure and biasing arrangement, the eFuse programming voltage can be kept below junction breakdown, ranging typically from 3-6V. Exemplary operating bias for the eFuse structures of Figures 2A, 3A, and 4A is shown in tabular format in Figure 5B.

During the Read mode of operation, with the biasing conditions established as described in the table of Figure 5B, the eFuse exhibits one of two predetermined responses in accordance with charge on the floating gate 215. When the floating gate 215 has been programmed (i.e., charged), it takes more voltage than a predetermined V_{ref} to turn on the floating gate transistor and thus no current will flow from source 210 to drain 211.

In contrast, when the floating gate 215 has not been programmed, V_{ref} is enough to turn on the isolation transistor 11 and the floating gate 12 transistor and current will flow from the source 210 to the bit line (i.e., drain 211). Current flow detection can then be used to determine the programming state.

To erase or reprogram, a negative programming voltage (in this example $-5V$) is applied to the control gate 216 and hence electrons are channeled away from the floating gate 215.

In another embodiment, illustrated in Figures 3A and 3B, the drain 311 is drawn with an extended RX width overlapping substantially all the floating gate 215. The extended RX width works the same as the isolated well 220 in that it increases drain-to-floating gate overlap to increase capacitive coupling thus enabling lower programming voltages. In a further embodiment, to increase the coupling efficiency of the drain voltage to the floating gate, the eFuse includes a drive-in implant formed in the semiconductor substrate as shown in Figures 4A and 4B. Although the drive-in implant 410 is shown in the extended drain configuration, it can also be used with the isolated well configuration.

Referring now to Figure 6A there is illustrated a fuse cell 610 in accordance with exemplary embodiments of the present invention. The fuse cell 610 includes an eFuse 200, select circuitry 615, latch circuitry 620, a programming transistor (Prog) 625, and a programming current source (OSC) 630. Since Flash programming involves high current injection, a HV source (OSC) 630 is needed to pass the required program current to BL (drain). The OSC 630 is coupled to the drain 211 of the 2-transistor eFuse 200 via Prog 625. Prog 625 is selected ON for programming and selected OFF for reading. The select circuitry 615 is coupled to the control gate 216 of the eFuse 200 for selecting the fuse for programming. Selection of the fuse is thru latch circuitry 620 to BL (drain) and select circuitry 615 to WL (gate). Latch and select circuitry can be connected to a state machine for command. Operation of the fuse cell may be understood by those skilled in the art with reference to the above-mentioned eFuse structure and the biasing conditions shown in Figure 6B. In particular, for programming, the source 210 is grounded and programming voltage of 5V is applied to the drain 211, 311 or bit line connection with Prog selected ON.

Figure 7 illustrates an array configuration using the eFuse shown in Figure 6A in which the select blocks 615 represent the select circuitry 615 of WL in Figure 6A and the latch blocks L1, L2, . . . LN represent the latch circuitry 620 to respective bit lines. The programming transistor 625 and OSC 630 have been omit for clarity.

Although a preferred embodiment of the method and system of the present invention has been illustrated in the accompanied drawings and described in the foregoing Detailed Description, it is understood that the invention is not limited to the embodiments disclosed,

but is capable of numerous rearrangements, modifications, and substitutions without departing from the spirit of the invention as set forth and defined by the following claims.